



230731 – DIGITAL NANO ELECTRONIC DESIGN

Credits: 5 ECTS

LECTURER

Coordinating lecturers: Jordi Madrenas, Jordi Cosp

Other lecturers: Francesc Moll

PRIOR SKILLS

Basic MOS models.

Electronic circuit design with MOS transistors.

Combinational and sequential digital design.

VHDL/Verilog design basics.

Basic VLSI design: Fabrication process, Basic layout, CMOS logic gates, DC and dynamic characteristics.

DEGREE COMPETENCES TO WHICH THE SUBJECT CONTRIBUTES

Specific:

- Design digital and analog CMOS integrated circuits of medium complexity.
- Apply low consumption techniques for integrated circuits (ICs).
- Design for testability and develop test schemes for ICs.

Transversal:

FOREIGN LANGUAGE: Achieving a level of spoken and written proficiency in a foreign language, preferably English, that meets the needs of the profession and the labour market.

TEACHING METHODOLOGY

- Lectures
- Laboratory sessions
- Laboratory practical work
- Short answer test (Control)
- Extended answer test (Final Exam)



LEARNING OBJECTIVES OF THE SUBJECT

Learning results of the subject:

- Understand the evolution of embedded technologies.
- Identify the cases and applications in which the realization of an integrated solution is convenient.
- Analyze the characteristics of a digital integrated circuit.
- Design CMOS digital integrated circuits of medium complexity.

STUDY LOAD

Hours large group: 26

Hours small group: 13

Hours self study: 86

CONTENTS

1 Introduction

- 1.1 State of the art in VLSI.
- 1.2 Moore's Law. CMOS limits and technology trends.
- 1.3 Technologies for digital design. Design process.
- 1.4 Cost performance tradeoff. Design space.
- 1.5 SoC. Chip examples.

Full-or-part-time: 4h

Theory lectures: 2h

Self study : 2h

2 Transistor and circuit models

- 2.1 Models of micro and nanoscale transistors for digital design.
- 2.2 Delay models.
- 2.3 RC delay model.
- 2.4 Linear model.
- 2.5 Logical effort.

Full-or-part-time: 8h

Theory lectures: 4h

Self study : 4h

3 Combinational circuit design

- 3.1 Structure of CMOS static gates.
- 3.2 Layout of CMOS static gates. Euler path method.
- 3.3 Propagation and contamination delay estimation.



3.4 Circuit families: Static, Ratioed circuits, CVSL, Dynamic circuits, Pass-transistor circuits.

3.5 Structured design strategies. Hierarchy, Regularity, Modularity, Locality.

3.6 Arithmetic blocks. Binary adders and multipliers.

Full-or-part-time: 18h

Theory lectures: 8h

Self study : 10h

4 Sequential circuit design

4.1 Latches and flip-flops. Setup and hold time.

4.2 Delay constraints. Clock skew.

4.3 Reset. E and T flipflops.

4.4 Counters, LFSRs and shifters. FIFO.

4.5 Synchronizers. Timing analysis. Slack. Clock domain crossing.

4.6 Integrated memory: SRAM, DRAM, ROM and Flash.

Full-or-part-time: 10h

Theory lectures: 4h

Self study : 6h

5 Power dissipation

5.1 Power dissipation sources.

5.2 Low-power design.

5.3 Dynamic power reduction. Clock gating.

5.4 Static power reduction. Power gating.

Full-or-part-time: 5h

Theory lectures: 2h

Self study : 3h

6 Practical aspects of VLSI design

6.1 Interconnect modeling. R, C, L. Skin effect.

6.2 Interconnect delay and energy.

6.3 Crosstalk.

6.4 Robustness and variability. Variability strategies.

6.5 Design corners.

6.6 Power supply distribution.

6.7 Clock distribution. Buffering.

6.8 Input/output pads.

6.9 Packaging.

Full-or-part-time: 6h

Theory lectures: 2h

Self study : 4h

7 Basic concepts of testing

7.1 The need of manufacturing test. Defects and faults.

7.2 Fault models. Yield. Test vectors.

7.3 Fault coverage. Controllability and observability.

7.4 Automatic Test Pattern Generation (ATPG). Delay fault testing.

7.5 Design for test (DFT).



- 7.6 Scan-based test.
- 7.7 Fault tolerance and self test. BIST.
- 7.8 System-level test.

Full-or-part-time: 9h
Theory lectures: 4h
Self study : 5h

Laboratory

Project design of a medium-complexity integrated circuit. CAE tools: simulation, synthesis and back-end. Layout design. Memory block. Standard cell library. Functional and back-annotated simulation.

Full-or-part-time: 39h
Laboratory sessions: 13h
Self study : 26h

GRADING SYSTEM

- Midterm and final exams (written tests for knowledge acquisition control): 50 % - 70 %
- Laboratory work: 30 % - 50 %

BIBLIOGRAPHY

Basic:

- Weste, N.H.E.; Harris, D.M. CMOS VLSI design: a circuits and systems perspective. 4th ed. Boston: Addison Wesley, 2011. ISBN 9780321547743.

Complementary:

- Lin, Ming-Bo. Introduction to VLSI systems: a logic, circuit, and system perspective. Boca Raton: CRC Press, 2012. ISBN 9781439868591.
- Jan Rabaey. Low Power Design Essentials. Springer, 2009. ISBN: 978-0-387-71713-5.
- Samar K. Saha, FinFET Devices for VLSI Circuits and Systems, CRC Press, 2020. ISBN 0429998090.