UNIVERSITAT POLITÈCNICA DE CATALUNYA
BARCELONATECH
Escola Tècnica Superior d'Enginyeria de Telecomunicació de Barcelona

telecos BCN

230735 – HIGH-LEVEL DIGITAL DESIGN

Credits: 5 ECTS

LECTURER

Coordinating lecturer: Juan Manuel Moreno Aróstegui

Others: Jordi Madrenas Boadas

PRIOR SKILLS

- Digital design based on an RTL-level hardware description language (VHDL, Verilog, ...)

- Design and simulation of basic digital systems: combinational and sequential logic functions, arithmetic functions and finite state machines.

- Implementation and debugging of basic digital systems on configurable devices (FPGAs).

- Development of software applications based on a microprocessor/microcontroller.

- C programming language.

DEGREE COMPETENCES TO WHICH THE SUBJECT CONTRIBUTES

Specific:

- Analyze, design and implement hardware/software communication interfaces.

- Specify and develop information processing systems using hardware/software co-design techniques.

- Design and implement digital systems based on embedded systems (SOC) configurable with high-level description languages and CAE tools.

Transversal:

TEAMWORK. Being able to work as a member of an interdisciplinary team, either as a member or carrying out management tasks, in order to contribute to developing projects with pragmatism and a sense of responsibility, assuming commitments taking into account the available resources.

TEACHING METHODOLOGY

- Lectures

- Laboratory classes

- Laboratory practical work

- Individual work (distance)

- Extended answer test (Final Exam)

LEARNING OBJECTIVES OF THE SUBJECT

Learning results of the subject:

- Understand the implications of hardware/software co-design and the use of configurable integrated systems (SOC).

- Design and implement communication interfaces between programmable subsystems (microprocessor/microcontroller) and configurable subsystems (FPGAs).

- Understand the high-level design principles of digital systems based on programmable and configurable components.

- Design and implement, using high-level design languages and techniques, digital communication and information processing systems.

STUDY LOAD

Hours large group: 26

Hours small group: 13

Hours self study: 86

CONTENTS

1. Introduction
- **1.1.** Principles of hardware/software codesign
- **1.2.** High-level synthesis methodology
- **1.3.** Design optimization principles
- **1.4.** High-level hardware description languages
- **1.5.** Architectures of configurable integrated systems

Full-or-part-time: 4 h.
Theory classes: 2 h.
Self study: 2 h.

2. High-level hardware description languages
- **2.1.** SystemC hardware description language
  - **2.1.1.** Functional modeling
  - **2.1.2.** Interfaces and channels design
  - **2.1.3.** Transaction-level modeling
  - **2.1.4.** Verification and debugging
- **2.2.** SystemVerilog hardware description language
  - **2.2.1.** Data types
  - **2.2.2.** Procedural blocks, tasks and functions
  - **2.2.3.** Interfaces
  - **2.2.4.** System verification primitives
  - **2.2.5.** Object-oriented programming
  - **2.2.6.** Threads and inter-process communication

Full-or-part-time: 15 h.
Theory classes: 6 h.
Self study: 9h.

3. **High-level digital synthesis**
   - **3.1.** Bit accurate data types
   - **3.2.** Data flow graph analysis
   - **3.3.** Resource allocation
   - **3.4.** Scheduling
   - **3.5.** Loop unrolling

   Full-or-part-time: 12 h.
   Theory classes: 6 h.
   Self study: 9h.

4. **Hardware/software interfaces**
   - **4.1.** Principles of hardware/software communication
   - **4.2.** On-chip buses
   - **4.3.** Microprocessor interfaces
   - **4.4.** Hardware interfaces

   Full-or-part-time: 22 h.
   Theory classes: 2h.
   Self study: 20 h.

5. **Design of custom processing subsystems**
   - **5.1.** Video subsystems
   - **5.2.** Vector and matrix multiplication
   - **5.3.** Sorting algorithms

   Full-or-part-time: 22 h.
   Theory classes: 2h.
   Self study: 20 h.

Laboratory:

- Configuration of a 32-bit microprocessor IP on an FPGA
- Design of custom communication and information processing subsystems
- Co-simulation and system integration

Full-or-part-time: 39 h.
Laboratory classes: 13 h.
Self study: 26 h.

GRADING SYSTEM

- Final exam: 40 %
- Collective works: 20 %
- Laboratory sessions: 40 %

BIBLIOGRAPHY

Basic:

- Patrick R. Scaumont, "A Practical introduction to Hardware/software Codesign", 2nd. Edition, Springer, 2013.

- Michael Fingeroff, "High-Lvel Synthesis Blue Book", Xlibris US, 2010.

- Ryan Kastner, Janarbek Matai, Stephen Neuendorfer, "Parallel Programming for FPGAs", open-source book, https://kastner.ucsd.edu/hlsbook/, 2018.

Complementary:

- T. Grötker, S. Liao, G. Martin, S. Swan, "System Design with SystemC", Kluwer Academic Publishers, 2002.

- S. Sutherland, S. Davidmann, P. Flake, "SystemVerilog for Design. A Guide to Using SystemVerilog for Design and Modeling", 2nd edition, Kluwer Academic Publishers, 2006.